Paving the way for future generations of smart sensors

Key benefits

- Single chip vision system embedding in-pixel processing circuitry allowing complex image sensing and processing at multi-thousand frames per second (fps)
- CMOS programmable Vision System on Chip (VSoC) optimized for industrial applications requiring image sensing, image processing, and decision making at extreme frame rates
- QCIF high speed image sensor processor
- Active pixels: 176 x 144
- On chip 32-bit RISC microprocessor for device control and image post processing
- On chip RAM for program and image/data storage
- Point to point, morphological, and statistical operations
- Spatial filtering, blob analysis and features extraction
- <2W power consumption @ 10,000fps (processing-dependent)

Features

- Global shutter
- Multiple communication ports including UART, PWM (2 ports), USB2.0, JTAG, and several software configurable general purpose input/output ports for controlling external devices like illumination sources or engines
- 1cm² packaged size with 700mW power consumption at full speed operation

Typical applications

- Automotive
- Machine vision
- Security
- Games
- Battery powered products
Sensor overview

The Eye-RIS Vision System on Chip (VSoC) is a programmable, autonomous, and complete VSoC using Teledyne AnaFocus’ proprietary and patented Smart Image Sensor (SIS) technology. SIS technology extends the functionality of CMOS image sensors with the incorporation of image storage and advanced mixed signal processing capabilities per pixel. Thanks to this technology, Eye-RIS VSoC delivers image processing capabilities and speed comparable to a high end conventional vision system, yet in a compact size with low power consumption.

The Eye-RIS VSoC is an autonomous device combining a parallel CMOS image sensor processor with 32-bit RISC microprocessor performing post processing and system control tasks, several I/O and high speed communication ports that allow the system to communicate and/or to control external systems, and on chip memory. The combination of massive parallel image pre-processing in the sensor with complex image post processing in the microprocessor results in ultra compact implementation of a vision system able to perform complex machine vision algorithms at speeds of several thousands of images per second. The Eye-RIS VSoC features a complete application development software environment allowing easy control of the device and is optimized for industrial applications requiring image sensing, image processing, and decision making at extreme frame rates.

Sensor characteristics

### Optical specifications

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<table>
<thead>
<tr>
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<tbody>
<tr>
<td>Image sensor</td>
<td>1cm² SIS CMOS</td>
</tr>
<tr>
<td>Sensing area</td>
<td>4.8 (h) x 5.9 (v) mm</td>
</tr>
<tr>
<td>Cell size</td>
<td>33.6μm (SQ)</td>
</tr>
<tr>
<td>Pixel active area</td>
<td>6μm (SQ)</td>
</tr>
<tr>
<td>Active pixels</td>
<td>176 x 144</td>
</tr>
<tr>
<td>Responsivity (DN8bits/ (μJ/cm²) @ 650nm (Max))</td>
<td>3.2</td>
</tr>
<tr>
<td>Dynamic range (dB)</td>
<td>52</td>
</tr>
<tr>
<td>PRNU</td>
<td>1.2%</td>
</tr>
<tr>
<td>DSNU</td>
<td>0.35%</td>
</tr>
<tr>
<td>Digital video output</td>
<td>Monochrome, 8 bits</td>
</tr>
<tr>
<td>Programmable exposure</td>
<td>1μs to 20ms</td>
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### In-pixel processing

- Storage of up to 7 gray level images and 4 binary images
- Gray scale image arithmetic, image convolutions, and scale to binary conversion
- Low pass, high pass, band pass, and stop band spatial filters with programmable bandwidth
- HitAndMiss binary operations (3x3 binary pattern matching)
- Active pixel detections
- RoI based processing

### On chip digital control and memory

- Altera Nios II 32-bit micro-processor
- JTAG module
- 8+8k bytes of instruction and data cache
- SPI interface for flash memory connection

### On chip digital control and memory continued

- 256k bytes of SDRAM for program and data
- Extension port for external SDRAM
- 128k bytes of SDRAM for image storage

### I/O and interfaces

- On chip bank of 4ADCs and 4DACs (8-bit at 50MHz) for gray-scale image I/Os
- Specific compressed I/O modes: image mean, number of pixels, coordinates of pixels
- 16-bit GPIO x2 PWM ports
- UART
- FIFO interface for image and data I/O

### Miscellaneous

- Power supply: Dual 3.3V and 1.8V
- Power: <2W @ 10,000fps (processing dependent) acquiring and reading out images to external memory. USB interface and 4GPIOs are considered to be active
- Operating humidity: 20 – 80% non-condensing
- Storage temperature/humidity: -10° to 60°C/20 – 80%

### Package

- 218 pin LGA, ceramic